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... reuse, • configuration statements for configuring **design** structure, • generate ... **Verilog**. ... to parameterize models by overloading **parameter** constants, there is ...
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J Jennings, E Beuscher - Proceedings of the 2nd conference on Domain-specific ..., 2000 - portal.acm.org
... **Verilog** has a small macro language, essentially based ... Therefore, although many **designs** are **parameterized**, there are ... Common **design** ele- ments in digital systems ...
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Parameterized IP core **design**
Z Junchao, C Weiliang, W Shaojun - ASIC, 2001. Proceedings. 4th International Conference on, 2001 - ieeexplore.ieee.org
... They are common in the **design** of the control Page 3 ... needs IF providers to support both **Verilog** and VFIDL ... For example, a **parameterized** IF core is designed to ...
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Increasing **design** quality and engineering productivity through **design** reuse - group of 2 »
E Girczyc, S Carlson - Proceedings of the 30th international conference on **Design** ..., 1993 - portal.acm.org
... Next, **designs** can be **parameterized**. While a ... In an FILD methodology, functionality can also be **parameterized** without increasing **design** cost if ...
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Three decades of HDLs. II. Conlan through **Verilog** - group of 6 »
D Borrione, R Piloty, D Hill, KJ Lieberherr, P ... - **Design** & Test of Computers, IEEE, 1992 - ieeexplore.ieee.org
... in the mid-1 970s through the development of **Verilog** in the ... evaluate and write as- sertions either after the interface/ **parameter** list of a **design** entity or ...
Cited by 8 - Related Articles - Web Search

Synthesis and Scripting Techniques for Designing Multi-Asynchronous Clock Designs - group of 9 »
CE Cummings - SNUG-2001 San Jose, CA Voted Best paper, 2001 - sunburst-**design**.com
... This time window is specified as a **design parameter** precisely to keep a data signal from changing too close to another synchronizing signal that could cause ...
Cited by 9 - Related Articles - View as HTML - Web Search

A System for Evaluating Performance and Cost of SIMD Array Designs - group of 14 »
MC Herbordt, J Cravy, R Sam, O Kidwai, C Lin - Journal of Parallel and Distributed Computing, 2000 - Elsevier
... program to generate the **designs** in the **Verilog** high-level ... 4. If a **design** to be evaluated has not ... thesized, but is legal for the **parameterized** hardware model ...
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Patent Search

Patents **1** - **10** of **21** on **verilog parameterized design**. (**0.00** seconds)

Mixed signal synthesis
US Pat. 6813597 - Filed Jun 8, 2000 - Cadence Design Systems, Inc.
Generate the **parameterized** model. i. **Parameterized** the circuit netlist.
2.2.1 Synthesis Models 2. Model each performance characteristic in terms of **design** ...

Mixed signal synthesis behavioral models and use in circuit **design** optimization
US Pat. 6637018 - Filed Oct 26, 2000 - Cadence Design Systems, Inc.
That is, Synthesis Plan is to formally record the **design** procedure so the synthesis model is '**parameterized**', that it is re-usable when the same circuit is ...

Apparatus and method for synthesizing integrated circuits using **parameterized** HDL modules
US Pat. 5841663 - Filed Sep 14, 1995 - VLSI Technology, Inc.
Kim ("Automatic behavioral **Verilog** model generation using engineering ...
and formal verification techniques for **parameterized** hardware modules", ...

Parameterized designing method of data driven information processor employing self-timed pipeline control
US Pat. 6546542 - Filed Jun 8, 2001 - Sharp Kabushiki Kaisha
The **design** flow in designing an LSI using the bottom up **design** procedure will
... for use with LSI designing (**Verilog**-HDL (Hardware Description Language), ...

CO X XX
US Pat. 7076415 - Filed Apr 28, 2000 - Cadence Design Systems
The **Verilog**-A/MS language is the modeling lan-guage—circuit-level models are ...
An example of a **parameterized** netlist (**design** parameters wnb, Inb, ibias, ...

Standard library generator for cell timing model
US Pat. 6496962 - Filed Nov 17, 2000 - LSI Logic Corporation
To migrate a circuit **design** to a new technology requires manually updating the
30 **Verilog** model library. The manual effort required for devel-oping and ...

Automatic code generation for integrated circuit **design**
US Pat. 6996799 - Filed Aug 8, 2000 - Mobilygen Corporation
The token bus specification can be **parameterized**. ... 4 and 5 are used in
conjunction with a template HDL (eg **Verilog**) file for Atom qa ...

Software tool to allow field programmable system level devices
US Pat. 6272451 - Filed Jul 16, 1999 - Atmel Corporation
System Designer seamlessly integrates Atmel's FPGA **design** tools and a third party
hardware (**verilog**/VHDL) simulator with its AVR microcontroller instruction ...

Circuit **design** method and apparatus supporting a plurality of hardware **design** languages
US Pat. 6226780 - Filed Aug 31, 1998 - Mentor Graphics Corporation
... "HDL Generation From **Parameterized** Schematic **Design** System," IEEE, pp.-,.* Sauge
et al., "Integrating of **Verilog**-HDL and VHDL Languages in the SMASH™ ...

Methods and apparatus for implementing parameterizable processors and peripherals
US Pat. 6976239 - Filed Jun 12, 2001 - Altera Corporation
Auser can also select to custom **design** a peripheral using various wizard pages.
... Con-ventional hardware description languages such as **Verilog** or VHDL ...